Title: METHOD AND SYSTEM FOR DYNAMICALLY

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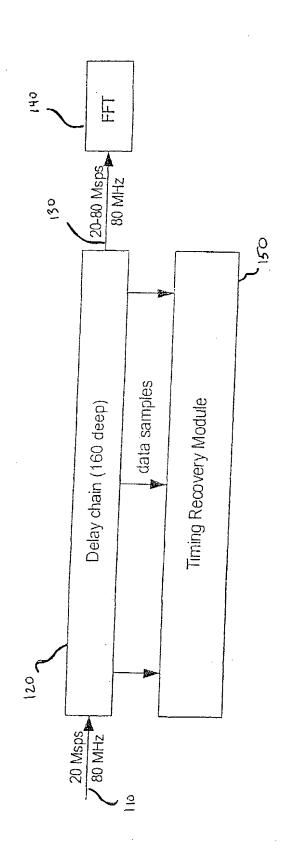
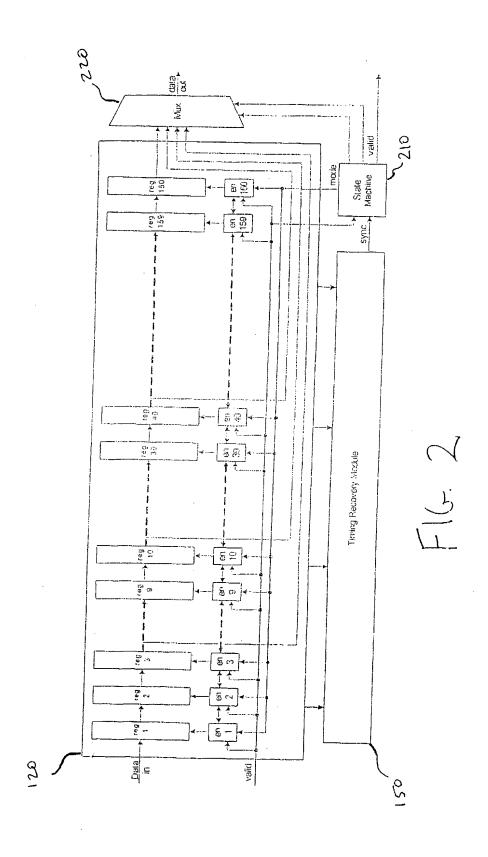
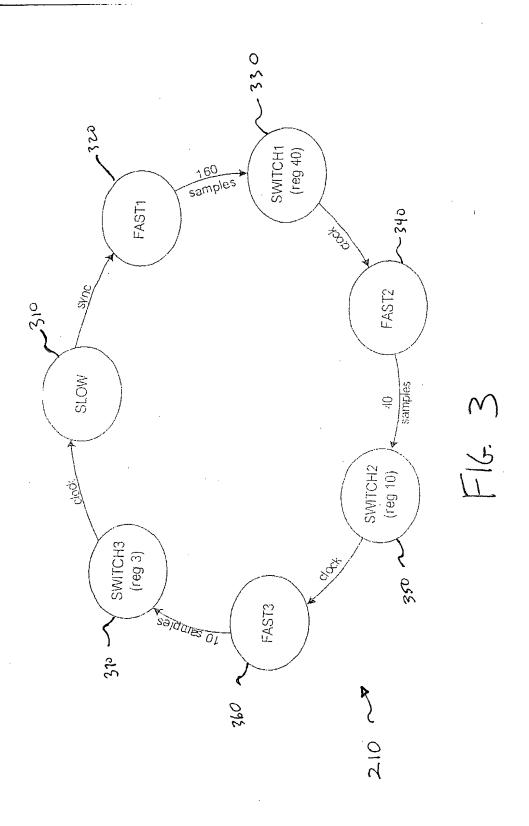


Figure 1

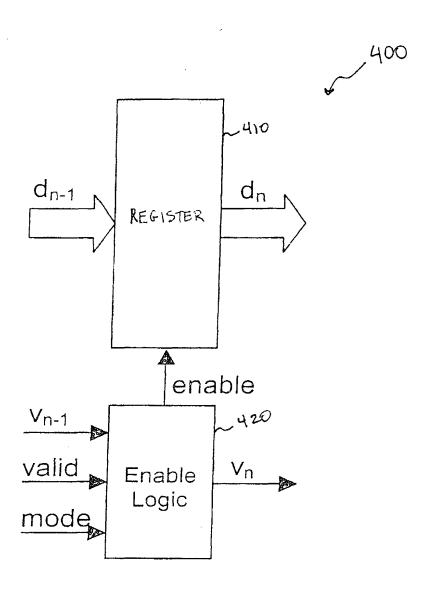
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F16. 4

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	Clock	Valid Signal (Incoming Sample at Delay Chain Input)	REGISTERS																	
	Cycle		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
SLOW	1		+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	÷	+	+
mode	2	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+
FAST mode	3		+	+_	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+
	4			+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+
	5				+	+	+	+	+-	+	+	+	+	+	+	+	+	+	÷	+
	6	+				+	+	+	+	+	+	+	+	+	+	+	+	+	+	+
	7		+	<u> </u>	<u>L</u> _	<u> </u>	+	+	+	+	+	+	+	+	+	+	+	÷	+	+
	8		+					+	+	+	+	+	+	+	+	+	+	_+_	+	+
	9		+		L		<u> </u>		+	+	+	+	+	+	+	+	+	+	+	+
	10	+	+		<u>L</u>					+	+	+	+	+	+	+	+	÷	+	+
	11		+	+							+	+	+	+	+	+	+	+	+	+
	12		+	+								+	÷	+	+	+	+	÷	÷	+
	13		+	+									+	+	+	+	+	+	+	+ _
	14	+	+	+										+	+	+	+	+	+	+
	15		+	+	+										+	+	+	+	+	+
	16		+	+	+				[+	+	+	+	+
	17		+	+	+												+	+	+	+
	18	+	+	+	+					[+	+	+
	19		+	+	+	+													+	+
	20		+	+	+	+]													+

Fig. 5

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